

## PATENT APPLICATION

Sheet 1 of 5

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR  
APPLICANT'S INFORMATION DISCLOSURE  
STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.

200210154-1

APPLICATION NO.

CONFIRMATION NO.

APPLICANT

Elias Gedamu


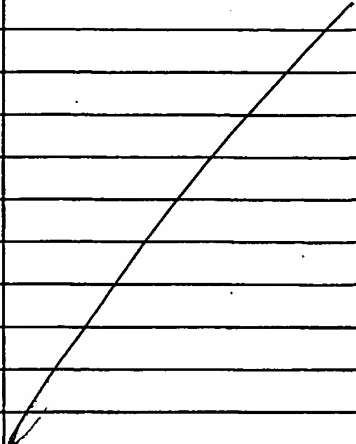

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1/15/2004

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## REFERENCE DESIGNATION

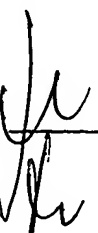


## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	1A	6,571,359	5/27/2003	Padwekar et al.	
	1B	6,523,151	2/18/2003	Hekmatpour	
	1C	6,484,275	11/19/2002	Josephson et al.	
	1D	6,430,705	8/6/2002	Wisor et al.	
	1E	6,427,224	7/30/2002	Devins et al.	
	1F	6,427,216	7/30/2002	El-Kik et al.	
	1G	6,385,740	5/7/2002	Treadway et al.	
	1H	6,385,552	5/7/2002	Snyder	
	1I	6,370,658	4/9/2002	Jeong	
	1J	6,363,509	3/26/2002	Parulkar et al.	
	1K	6,285,974	9/4/2001	Mandyam et al.	

## FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L				
	1M				
	1N				
	1O				
	1P				

## OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	1Q	Chen, Li and Sujit Dey, "Software-Based Self-Testing Methodology for Processor Cores," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 20, No. 3, March 2001 (pages 369-380).
	1R	Chen, Li, Sujit Dey, Pablo Sanchez, Krishna Sekar, and Ying Chen, "Embedded Hardware and Software Self-Testing Methodologies for Processor Cores," Los Angeles, CA, 2000 (6 pages).
	1S	Geotest, "Dynamic Testing of Micro-Processor Based Products," Santa Ana, CA (4 pages).

EXAMINER

DATE CONSIDERED

12/15/00



## PATENT APPLICATION

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<b>FORM PTO-1449</b>  <b>LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT</b>  (Use several sheets if necessary)	ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
	200210154-1		
	APPLICANT		
	Elias Gedamu		
	FILING DATE	GROUP	
	1/15/2004		

## REFERENCE DESIGNATION




## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	2A	6,212,667	4/3/2001	Geer et al.	
	2B	6,181,004	1/30/2001	Koontz et al.	
	2C	6,064,948	5/16/2000	West et al.	
	2D	6,055,649	4/25/2000	Deao et al.	
	2E	6,042,384	3/28/2000	Loiacono	
	2F	6,031,992	2/29/2000	Cmelik et al.	
	2G	6,028,983	2/22/2000	Jaber	
	2H	5,928,334	7/27/1999	Mandyam et al.	
	2I	5,884,023	3/16/1999	Swoboda et al.	
	2J	5,867,719	2/2/1999	Harris, II et al.	
	2K	5,862,366	1/19/1999	Schmidt et al.	

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	2L					
	2M					
	2N					
	2O					
	2P					

## OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	2Q	Johnson, David J. C., "HP's Mako Processor," Fort Collins, CO, October 2001 (16 pages).
	2R	Kranitis, N., A. Paschalis, D. Gizopoulos, and Y. Zorian, "Effective Software Self-Test Methodology for Processor Cores" (6 pages).
	2S	Kranitis, N., G. Xenoulis, D. Gizopoulos, A. Paschalis, and Y. Zorian, "Low-Cost Software-Based Self-Testing of RISC Processor Cores," 2003 (6 pages).

EXAMINER

DATE CONSIDERED

12/15/06

## PATENT APPLICATION

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LIST OF PATENTS AND PUBLICATIONS FOR  
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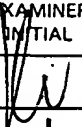

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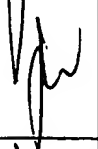

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	3A	5,841,968	11/24/1998	Caldera et al.	
	3B	5,699,506	12/16/1997	Phillips et al.	
	3C	5,673,274	9/30/1997	Yoshida	
	3D	5,673,272	9/30/1997	Proskauer et al.	
	3E	5,671,531	9/30/1997	Mugiya	
	3F	5,654,972	8/5/1997	Kuroiwa et al.	
	3G	5,638,382	6/10/1997	Krick et al.	
	3H	5,623,499	4/22/1997	Ko et al.	
	3I	5,617,531	4/1/1997	Crouch et al.	
	3J	5,596,583	1/21/1997	Krenik et al.	
	3K	5,590,134	12/31/1996	Yin	

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	3N					
	3O					
	3P					

## OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	3Q	Lai, Wei-Cheng and Kwang-Ting Cheng, "Instruction-Level DFT for Testing Processor and IP Cores in System-on-a-Chip," Santa Barbara, CA, 2001 (6 pages).
	3R	Silas, Isic, Igor Frumkin, Eilon Hazan, Ehud Mor, and Genadiy Zobin, "System-Level Validation of the Intel Pentium M Processor," Intel Technology Journal, Vol. 7, Issue 02, May 2003 (pages 37-43).
	3S	Singh, Virendra, Michiko Inoue, Kewal K. Saluja, and Hideo Fujiwara, "Software-Based Delay Fault Testing of Processor Cores" (10 pages).

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DATE CONSIDERED

## PATENT APPLICATION

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## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
K	4A	5,590,134	12/31/1996	Yin	
	4B	5,581,491	12/3/1996	Biwer et al.	
	4C	5,566,344	10/15/1996	Hall et al.	
	4D	5,487,169	1/23/1996	Vraney et al.	
	4E	5,444,716	8/22/1995	Jarwala et al.	
	4F	5,359,547	10/25/1994	Cummins et al.	
	4G	5,355,369	10/11/1994	Greenberger et al.	
	4H	5,233,612	8/3/1993	Huyskens et al.	
	4I	5,157,781	10/20/1992	Harwood et al.	
	4J	5,142,688	8/25/1992	Harwood, III	
	4K	5,128,737	7/7/1992	van der Have	

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	4L				
	4M				
	4N				
	4O				
	4P				

## OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

K	4Q	Ur, Shmuel and Yoav Yadin, "Coverage Driven Processor Test Generation: Proof of Concept," September 1997 (pages 1-16).
	4R	Kim, Hyungwon and John P. Hayes, "High-Coverage ATPG for Datapath Circuits with Unimplemented Blocks," Ann Arbor, MI (10 pages).
	4S	
EXAMINER		DATE CONSIDERED 12/15/06

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Sheet 5 of 5

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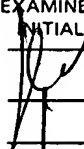
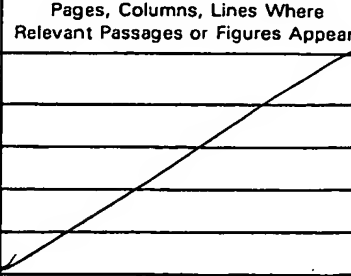

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## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	5A	5,119,379	6/2/1992	Dara	
	5B	5,067,129	11/19/1991	Evans et al.	
	5C	5,021,997	6/4/1991	Archie et al.	
	5D	4,707,848	11/17/1987	Durston et al.	
	5E	4,520,440	5/28/1985	Buonomo et al.	
	5F				
	5G				
	5H				
	5I				
	5J				
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12/5/06